**MEHRAN UNIVERSITY OF ENGINEERING AND TECHNOLOGY, JAMSHORO**

**DEPARTMENT OF ELECTRONIC ENGINEERING**

**DIGITAL ELECTRONICS**

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| **ROLL NO : 20ES062** | **SECTION : 02** |
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**COMPLEX ENGINEERING PROBLEM**

**CEP Statement**

Design an Automobile Parking Control that make the use of an up/down counter to solve an everyday problem. The problem is to devise a means of monitoring available spaces in a one-hundred space parking garage and provide for an indication of a full condition by illuminating a display sign and lowering a gate bar at the entrance.

# INTRODUCTION

Digital systems are created to perform data processing and control tasks. Architecture tailored is what distinguishes one system from another to efficiently execute the tasks for which it was designed. Today digital technologies are dominants because digital systems are easier to design, accurate and precise, also information are stored easily and portably in digital systems.The main building blocks of automobile parking control system are the sequential devices like up/down binary counters, combinational devices like logic gates. Others include seven segment LED displays for display and sensors. The up/down counter which is a negative edge triggered is operated using S-R latch or any other 555 timers that fits.

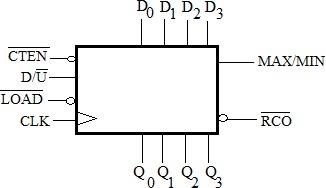
The 120 count was achieved by decoding the three cascaded up/down counters using basic logic gates such that for every 0 through 9 counts of the first counter the second counter is enabled via its terminal count to advance through its state from 0 through 9. Similarly, at terminal count of the second counter the third counter is allowed or enabled to advance through its state to count 1 which is its maximum number of counts. Once the third counter counts 1 while the second is at 2 and the first counter is at count 0 making a total of 120 counts the decoding gates becomes active and hold the counters at that 120 count. Each up count represents a detected car entering into the garage by the sensor placed at the entry likewise each down count represents a detected car leaving the garage by the sensor placed at the exit. Additional circuitries are required for these operations especially at the entry when the garage is fully occupied at 120 counts and at the exit when the garage is empty at 000 counts. In all these sections the operations are displayed using seven segment displays to show the respective counts. Finally all these sections; the counter section, sensor section, S/R latch section and display section are then connected together to form the design of the complete system. The design was carried out and implemented using simulation software’s multisim version 11 and proteus

However, the project is limited for only 120 cars into a 120 parking garage, the project is mainly for public and private parking where many cars up to 120 are expected to be parked, the sensors are designed to detect only cars, the barrier at the gate will remain opened (raised) until the counter counts 120 then it will be lowered to block further entry.

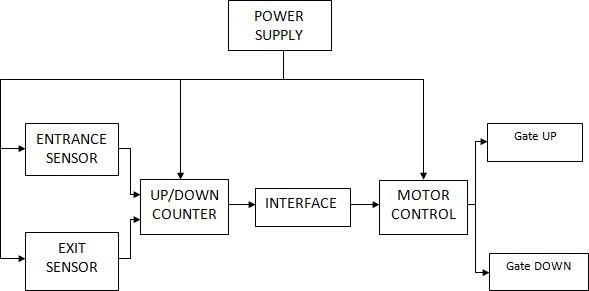
# UP/DOWN COUNTER

An up/Down counter also called a bidirectional counter is a counter capable of progressing in either direction through a certain sequence. It can have any specified sequence of states. The up/down counter also come in integrated circuit(IC) form. One good example of this counter is 74HC190 type which counts in both directions. The direction of the count is determined by the level of the up/down input D/. When this input is

HIGH the counter counts down and when the input goes LOW the counter counts up. It is BCD counter (Decade) hence counts (0000) through (1001) (Floyd, 2009; Bolton, 2004). D0 through D3 and Q0 through Q3 are the data inputs and outputs respectively, also this device can be preset to any desired BCD digit using LOW level at input. Figure 3 is the 74HC190 up/down decade counter.

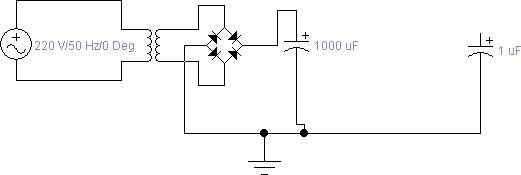
Figure 3: 74HC190 up/down decade counter

# BLOCK DIAGRAM OF PARKING SYSTEM:



1. **POWER SUPPLY UNIT**

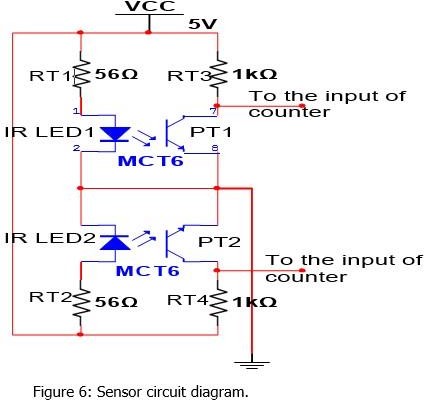
For perfect operation of any digital device it is necessary to provide stable power supply that serve as SET when turned ON and RESET when turned OFF. The accepted technical specification for CMOS used for this design is between 2.5 V to 5 V, likewise this design employed the use of 74XX series CMOS (Kleitz, 2006; Galadanci, et al. 2013). The a.c supply is chosen to be 220/240 V, 60Hz connected to the input of the transmitter which step it down to 12V at secondary terminal. A bridge rectifier was used for full rectification or simply conversion of a.c to d.c the capacitors were selected for good filtering of harmonics, ripples or unwanted signals. After having smooth 12V d.c the 7805 voltage stabilizer was used to stabilize the voltage at 5v as reguired by the design. Also a 5V d.c battery can be used for this application. Figure 5 is the circuit diagram of the power supply unit.



7805

# SENSOR UNIT

Sensors plays an important role in this design; the sensor used is phototransistor opto-coupler which is one of the types of opto electronics sensors comprise of Light emitting diode (LED) and photo transistor. This device is capable of detecting object and producing an electrical signal that is proportional to the amount of light incident on the active area of the device. As seen in Figure 6, there are two sensors placed at both the entry and the exit (Floyd, 2009; Karim and Chan, 2008; Myke, 2005). The light emitting diode (LED) at the entry IR LED1 continuously transmit an infrared signal which is directly facing the photo transistor PT1, this transistor conducts as a result of light indented on it by the LED, as such the collector of the transistor PT1 is in LOW state. The phototransistor opto-coupler is connected in the dark activation so that when a car passes through the entry gates the infrared light is interrupted and the photo transistor PT1 stop conducting, providing a HIGH signal to the S input of the S-R latch, and hence allows the counter to advance through it state by increment its count. The operation of the Exit sensor is similar to that of entry sensor only that when a car passes through the exit sensor (IR LED2, PT2) placed at the exit gate the photo transistor stop conducting and provide HIGH signal to R input of the S-R latch which causes the counter to decrement its count (Kleitz, 2003; Scherz, 2000).



# COUNTER UNIT

The counting section of this project was designed by cascaded arrangement of three decade up/down counter. The 1st counter counts from 0 to 9 and then recycle to 0 for all the sequences and the 2nd counter counts from 0 to 9 and recycles to 0 through all the required sequence, similarly it also advances from 0 to 2 on the last cycle. The principle of operation of the 2nd counter is that it only advances whenever the 1st counter goes from 0 through to 9. The 3rd counter remain at count 0 until the 1st and 2nd counters count 99 simultaneously then on next clock pulse that recycles both the two counters to 00 the 3rd counter advances to 1 there by making the hundredth count (Floyd, 2009; Karim, 2008; Tokheim, 2006; Bolton. 2004). The Ripple clock output (RCO) of the 1st counter was connected to the count enable input (CTEN) of the 2nd counter and the Ripple clocking Output (RCO) of the 2nd counter was connected to the count enable input (CTEN) of the 3rd counter as shown in Figure 7. On the clock pulse that recycles the 1st counter from 0 back to 9 (as indicated on its display D1), its RCO goes LOW and hence activates the enable input CTEN of 2nd counter to show 1 on its display D2. This process continued until the maximum count is exhausted. Likewise, CTEN of the 3rd counter is enabled when RCO of the 2nd counter is LOW on its 9 to 0 transition to display count 1 from its display D3 (Galadanci et al., 2013). The S-R latch marked (0) was used because the counters are negative, that is LOW signal from S input put the counter into UP count mode while HIGH signal from R input put the counter into a DOWN count mode. That is why the negative output of the S-R latch () is connected to the /DOWN terminals of the counters. NOR gate G1 receives its inputs from the exit and entry sensors in such a way that when a car passes through either of the gates, the sensor placed at that gate will be active and send HIGH signal to the NOR gate in order to produce a HIGH to LOW clock pulse transition at its output which is connected to the clock inputs of all the counters.

**METHOD**

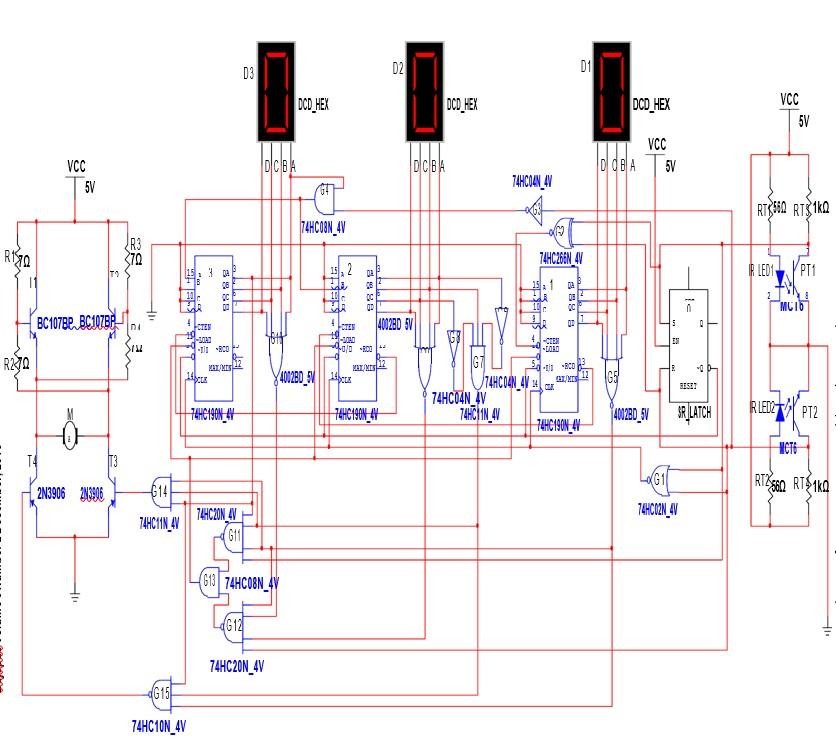
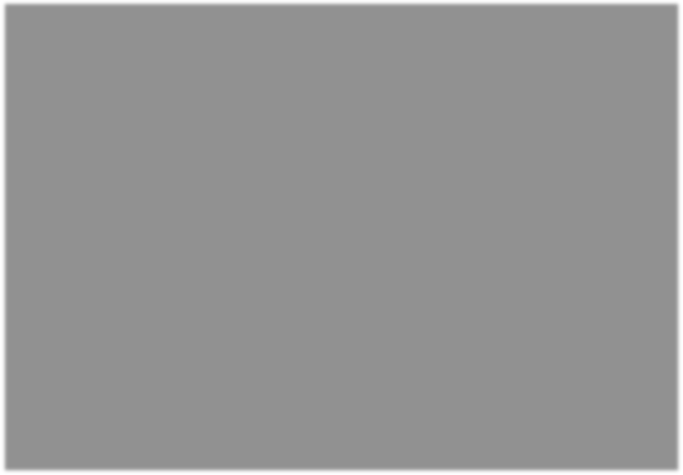
An automobile parking control system is one of the types of digital binary counter applications.

# CIRCUIT DIAGRAM

The general circuit is shown in Figure 9 consisting of the three units already discussed; the sensor unit, counter unit and motor circuit section. The entrance sensor MCT6 detect the presence of a car by interrupting the transmitted infrared light from photo diode (IR LLED1) to photo transistor PT1 and send a HIGH signal to the S input of the S-R latch marked (0). The S-R latch produce a LOW signal at its output which is directly connected to the /down inputs of all the three counters and increment the counters in up count, these count continues base on the number of cars (pulses send from entrance sensor) that enter the parking lot.The Exit sensor has the same operation as similar to that of entrance only that it detects the presence of cars leaving the garage; and sent a HIGH signal to the R input of S-R latch to produces HIGH signal through its output which causes the counter to decrement.

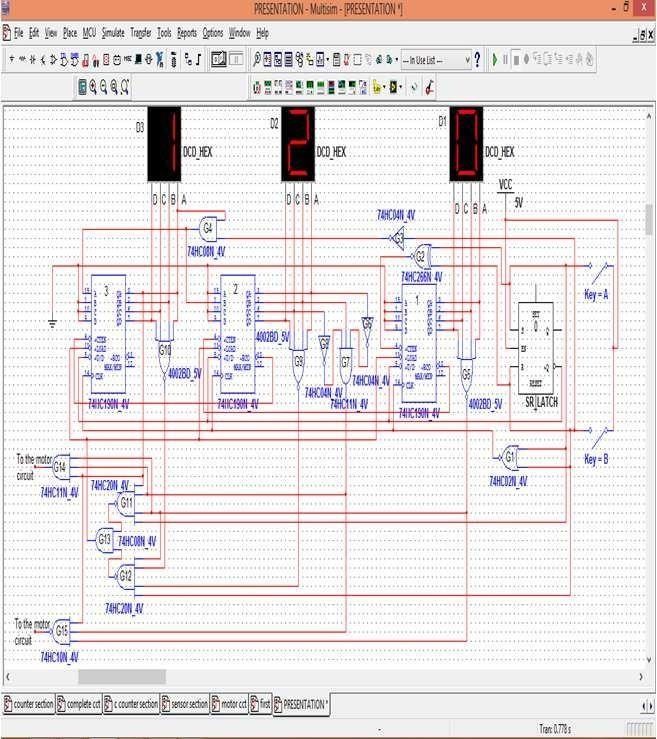
# MODE OF OPERATION OF CIRCUIT DIAGRAM

The mode of operation is based on the working principle of all the previously designed sections. As can be seen from the general circuit diagram of Figure 9 at each entry or exist of an individual vehicle the counters decrement the count until all the cars are parked in or out of the garage. The gate G1 provide a HIGH to LOW clock pulse whenever a car enters or leaves the garage having its inputs tapped from both the entry and exit sensors while its output goes to the clock input CLK of all the counters. The gate G2 allow the counter not to count up or down; that is whenever a car is entering and another car is leaving the garage at the same time, G2 force the counters to remain in their previous state. Also its inputs are tapped from both sensors at the gates and its output is linked to the count enable input CTEN of the first counter(1) which is the primary counter, meaning when the CTEN input of this counter receives a HIGH signal none of the counters will be active. The 1st counter count from 0 to 9 but at the pulse that recycles it from 9 back to 0, its ripple clock output RCO goes LOW which enables count enable of the 2nd counter. This counter advances through its state sequence at each 9 back to 0 clock pulse of the 1st counter until it reaches 9 where on the next clock pulse the ripple clock output of the 2nd counter will be LOW, activating the 3rd counter through its active LOW count enable input CTEN to count one (1). The 1st counter has to count continuously from 0 to 9 twice to make the 3rd counter to display 1 and the 2nd counter to display 2 on the 9 to 0 clock pulse of the 1st counter. This is the maximum 120 count displayed through the seven segment displays D3, D2 and D1 respectively. At this point G3 and G4 produces HIGH logic level to the A and B inputs of 3rd and 2nd counters while LOW logic level is applied to the inputs of the 1st counter. These inputs are loaded into the counters when G13 produces a LOW signal by activating the active LOW inputs of all the counters (Roger, 1994; Barry, 1998; Galadanci, et al.). In the up count gate G5 decode 0 from the 1st counter and gates G6, G7 and G8 decode 2 from the 2nd counter and a wire tapped from the least significant bit (LSB) of the 3rd counter to decode 1. These are connected to the inputs of gate G11. Likewise in the down count gates G5, G9 and G10 decode 0s from all the counters and their outputs are linked to the inputs of gate G12. But if either G11 or G12 produces LOW voltage at 120 or 000 counts respectively; G13 output go LOW and hence activate the LOAD inputs of the counters which load the available data inputs on their respective input terminals. The gates G14 and G15 are complementary gates. G14 always produces a HIGH signal only at 120 counts which activate the transistors T3 and T1 to drive the DC motor to rotate in anti- clockwise direction to block further entry. These indicate that there is no more available space for parking inside the garage. Gate G15 always produces a HIGH signal when a car moves out through the exit hence activate transistors T4 and T2 to drive the motor in the clockwise direction which open the gate for further entry.



The 3rd counter was considered as a hundredth counter (it counts in hundred) and the 2nd counter regarded as a tenth counter while the 1st counter considered to be the unit counter. The design was simulated using national instrument electronics software (multisim version 11.0). The other part of the design that consisted of the DC motor circuit where NPN and PNP were cross coupled to drive the motor in either direction was simulated using proteus software. Figure 10 and 11 shows pictorial diagram of both the counting part and motor circuit part respectively.

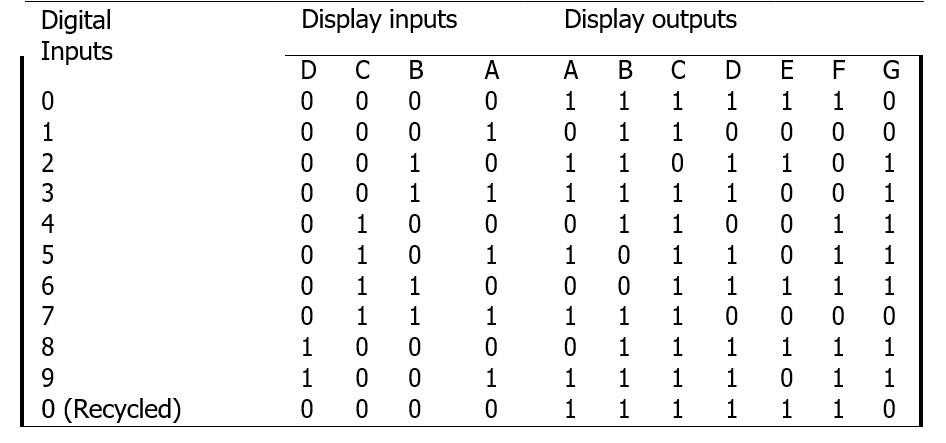
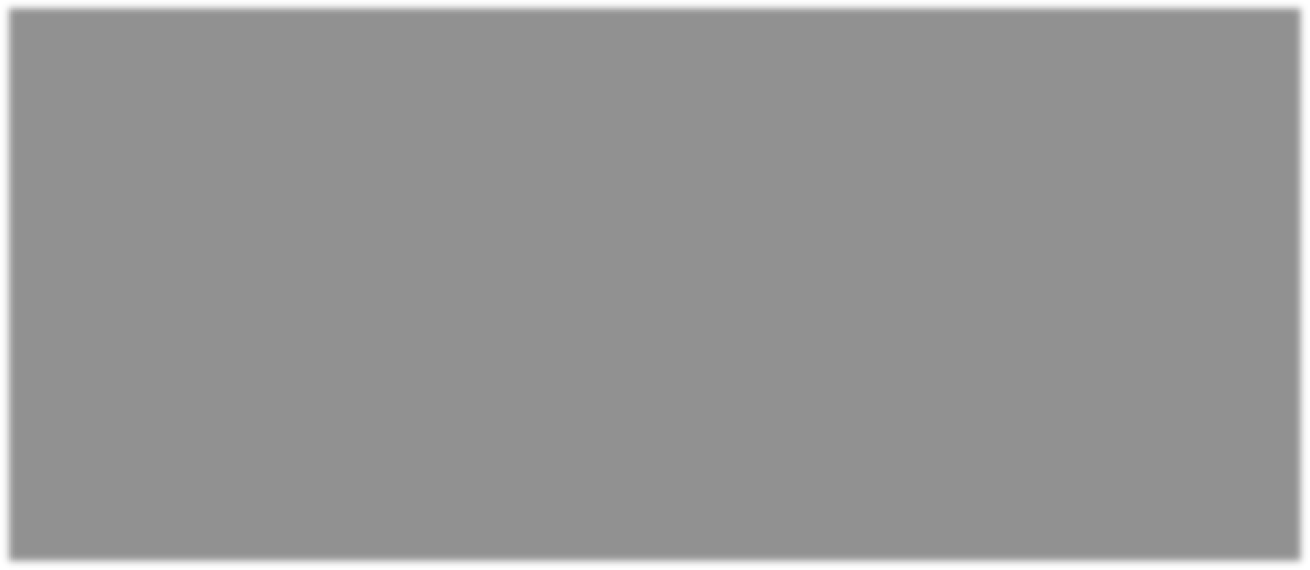
**SIMULATION RESULTS:**



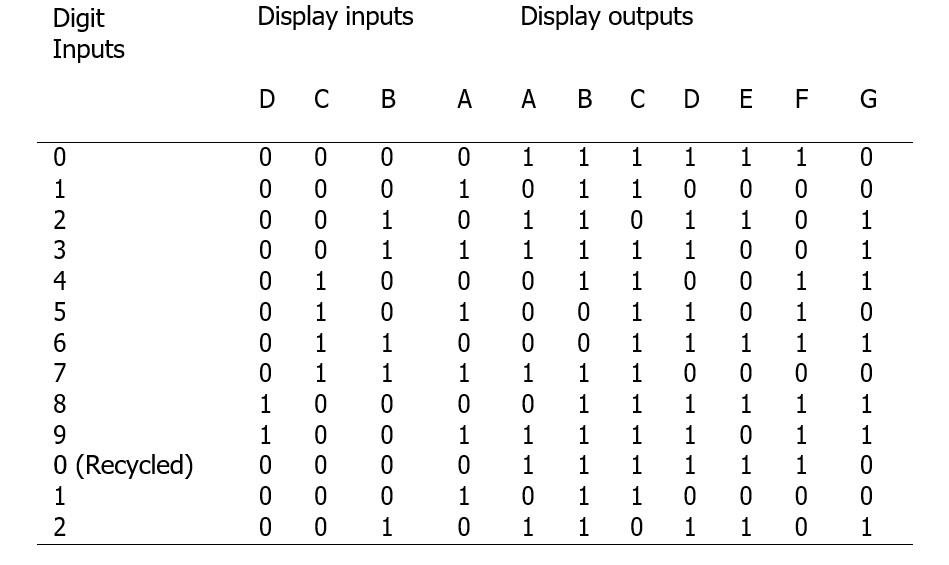
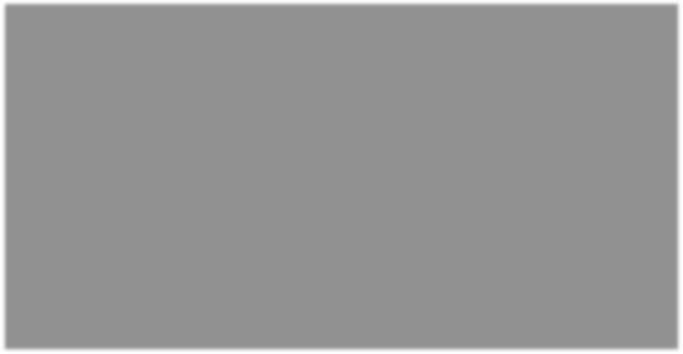
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# RESULTS AND DISCUSSIONS

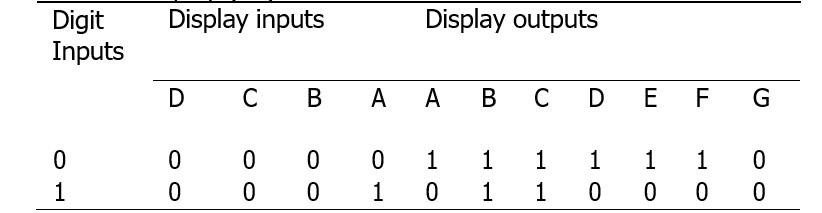
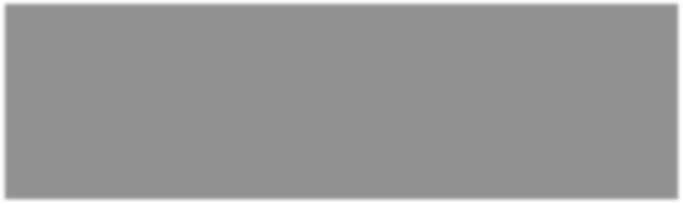
The aim of this work is to design 120 capacity automatic parking lots control system where 120 cars can be parked. After the simulation was completed, the number of counts (cars entering or leaving the garage) was observed from seven segment display of each counter. The DC motor was used to drive the gates closed or opened (anticlockwise or clockwise) when the garage is fully occupied or not. Table 3 shows the possible count display of the 1st, 2nd and 3rd counters. The 1st counter counts from 0 to 9 and recycle back to 0 for every single count of the 2nd counter. Table 3: Display (D1) of the 1st counter for every single count of 2nd counter.



But in case of the 2nd counter, it count from 0 to 9 and recycle back to 0 and also proceed to 2 as determined from its display D2 as shown in Figure 4. Table 4: Maximum count display (D2) of the 2nd counter



However, the count display of the 3rd counter is shown in Table 5, where it count 1 on the 9 to 0 clock pulse of the 2nd counter.



## CONCLUSION

In conclusion the design of 120 capacity automobile parking control system was successfully carried out using synchronous decade up/down counters and logic gates, sensor and DC motor. The design was implemented and simulated using proteus and multisim simulation softwares. The result of the simulation indicates that the system functions as desired, where if the full capacities of 120 cars are parked in the parking lot, the gate closes and waits for an available space before the gates open for additional cars to enter. The available space is always determined by the number of cars that leave the garage.

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